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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,754	11/15/2001	Darrell G. Hill	SC10776P D01	3259

23330 7590 03/25/2004

MOTOROLA, INC.
CORPORATE LAW DEPARTMENT - #56-238
3102 NORTH 56TH STREET
PHOENIX, AZ 85018

EXAMINER

MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/007,754

Applicant(s)

HILL ET AL.

Examiner

Victor A Mandala Jr.

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. The Applicant has amended independent claims 10 and 14 to read around previous rejection under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,392,258 Hirata et al. The examiner has considered the Applicant's amendments but finds them to still read on Hirata et al. The Applicant argues that Hirata et al. does not teach an exposed portion of the base layer is adjacent the emitter layer and the base contact. Hirata et al. does teach the limitation, which can be seen in Figure 3b, of the exposed portion of the base layer as being labeled by the examiner to be #300. The exposed portion #300 can be seen to be adjacent to the surface of the emitter layer, (examiner's label #400), and the base contact surface, (examiner's label #500). The Applicant also argues that in claim 14 Hirata et al. does not teach the base contacts to be spaced apart from the emitter layer. The examiner has also considered this argument but finds it to be non-persuasive because the base contact #9 is spaced apart from a majority of the area of the emitter layer #5 and also the center point of the layer #5. The claim does not mention the base contacts are laterally spaced apart from the *entire* emitter layer, thus allowing the examiner to interpret the claim in the broadest view. The 35 U.S.C. 102(e) rejection as being anticipated by U.S. Patent No. 6,392,258 Hirata et al. on claims 10 and 12-14 stands as is.

2. Newly added claims 15-18 will be examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10, 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,392,258 Hirata et al.

3. Referring to claim 10, a semiconductor component comprising: a semiconductor substrate, (Figure 3b #1), having an emitter layer, (Figure 3b #5), a base layer, (Figure 3b #4), and a collector layer, (Figure 3b #3), wherein the base layer, (Figure 3b #4), is over the collector layer, and the emitter layer has a surface passivation ledge, (Figure 3b examiner's label #100), disposed on the base layer, (Figure 3b #4); a dielectric layer, (Figure 3b #14), formed over the passivation ledge, (Figure 3b examiner's label #100); and a base contact, (Figure 3b #9), overlying a portion of the base layer, (Figure 3b #4), and overlapping onto the dielectric layer, (Figure 3b #14), whereby an exposed portion of the base layer, (Figure 3b examiner's label #300), is adjacent the emitter layer, (Figure 3b examiner label #400), and the base contact, (Figure 3b examiner's label #500).

4. Referring to claim 12, a semiconductor component, wherein a region of the base layer, (Figure 3b #4), and a region of the collector layer, (Figure 3b #3), form boundaries that are substantially aligned to a first edge, (Figure 3b examiner's label #200), of the base contact, (Figure 3b #9), that is remote from the emitter layer, (Figure 3b #5).

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5. Referring to claim 13, a semiconductor component, wherein the base layer, (Figure 3b #4), is comprised of a p type material, (Col. 2 Lines 20-21).

6. Referring to claim 14, a heterojunction bipolar transistor comprising: a substrate layer, (Figure 3b #1), a subcollector layer, (Figure 3b #2), a collector layer, (Figure 3b #3), a base layer, (Figure 3b #4), and an emitter layer, (Figure 3b #5), each layer formed on top of the preceding layer; an emitter mesa and a thin passivating ledge, (Figure 3b examiner's label #100), formed in the emitter layer, (Figure 3b #5); base contacts, (Figure 3b #9), depositing on the base layer, (Figure 3b #4), wherein the base contacts, (Figure 3b #9), are self aligned with respect to the passivating ledge, (Figure 3b examiner's label #100), and are laterally spaced apart, (see Response to Amendment), from the emitter layer, (Figure 3b #5).

7. Referring to claim 15, a HBT, further comprising: a dielectric layer, (Figure 3b #14), overlying at least a portion of the passivation ledge, (Figure 3b examiner's label #100).

8. Referring to claim 16, a semiconductor component comprising: a semiconductor substrate, (Figure 3b #1), having an emitter layer, (Figure 3b #5), a base layer, (Figure 3b #4), and a collector layer, (Figure 3b #3), wherein the base layer, (Figure 3b #4), is over the collector layer, (Figure 3b #3), and the emitter layer, (Figure 3b #5), has a surface passivation ledge, (Figure 3b examiner's label #100), disposed on the base layer, (Figure 3b #4); a dielectric layer, (Figure 3b #14), formed over the passivation ledge, (Figure 3b examiner's label #100); and a base contact, (Figure 3b #9), overlying a portion of the base layer, (Figure 3b #4), and overlapping onto the dielectric layer, (Figure 3b #14), wherein a portion of the dielectric layer, (Figure 3b examiner's label #600), is between the base layer, (Figure 3b #4), and the base contact, (Figure 3b #9).

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9. Referring to claim 17, a semiconductor component comprising: a semiconductor substrate, (Figure 3b #1), having an emitter layer, (Figure 3b #5), a base layer, (Figure 3b #4), and a collector layer, (Figure 3b #3), wherein the base layer, (Figure 3b #4), is over the collector layer, (Figure 3b #3), and the emitter layer, (Figure 3b #5), has a surface passivation ledge, (Figure 3b examiner's label #100), disposed on the base layer, (Figure 3b #4); a dielectric layer, (Figure 3b #14), formed over the pasivation ledge, (Figure 3b examiner's label #100); and a base contact, (Figure 3b #9), overlying a portion of the base layer, (Figure 3b #4), and overlapping onto the dielectric layer, (Figure 3b #14), wherein the base contact, (Figure 3b #9), is laterally spaced apart, (see Response to Amendment), from the emitter layer, (Figure 3b #5).

10. Referring to claim 18, a heterojunction bipolar transistor (HBT) comprising; a substrate layer, (Figure 3b #1), a subcollector layer, (Figure 3b #2), a collector layer, (Figure 3b #3), a base layer, (Figure 3b #4), and an emitter layer, (Figure 3b #5), each layer formed on top of the preceding layer; an emitter mesa, (Figure 3b #5), and a passivating ledge, (Figure 3b examiner's label #100), formed in the emitter layer, (Figure 3b #5); base contacts, (Figure 3b #9), deposited on the base layer, (Figure 3b #4), wherein the base contacts, (Figure 3b #9), are self aligned with respect to the passivation ledge, (Figure 3b examiner's label #100); and a dielectric layer, (Figure 3b #14), overlying at least a portion of the passivating ledge, (Figure 3b examiner's label #100), wherein a portion of the dielectric layer, (Figure 3b examiner's label #600), is between the base layer, (Figure 3b #4), and the base contact, (Figure 3b #9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,392,258 Hirata et al.

11. Referring to claim 11, a semiconductor component, wherein the dielectric layer, (Figure 3b #14), is comprised of a material selected from the group consisting of silicon nitride, aluminum nitride, silicon dioxide, silicon oxynitride, and mixtures thereof.

Hirata et al. discloses the claimed invention except for the dielectric layer comprising the materials as claimed in claim 11. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the dielectric layer out of the materials as claimed in claim 11 instead of a polyimide resin as taught by Hirata et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

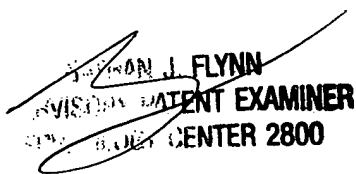
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
3/17/04


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